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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/544,392	04/06/2000	Kazunobu Kuwazawa	005317-20069	8777

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	09/544,392	KUWAZAWA, KAZUNOBU	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *35-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,12,16,28,29 and 32-34* is/are rejected.

7)☒ Claim(s) *4-11,13-15,17-27,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-34 in the response filed 4/11/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: MEMORY DEVICE AND DISSIMILAR CAPACITORS FORMED ON SAME SUBSTRATE.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 2 recites the limitation "the capacitor element" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Tsuruta et al.. Tsuruta et al. discloses a semiconductor device having a non-volatile memory transistor (col. 1, lines 19-20), comprising: a first capacitor element (col. 8, line 31) and a second capacitor element (col. 8, line 39), the non-volatile memory transistor, the first and the second capacitor element being formed in one semiconductor substrate (col. 3, lines 8-10), the first capacitor element including a first lower electrode, embodied as a lower conductive film (col. 8, line 32), a first dielectric film, embodied as an insulating inter-layer film (col. 8, line 33) and a first upper electrode, embodied as an upper conductive film (col. 8, line 34), the second capacitor element having a second lower electrode, embodied as a lower conductive film (col. 8, line 41), a second dielectric film, embodied as an insulating inter-layer film (col. 8, line 43) and a second upper electrode, embodied as a upper conductive film (col. 8, line 44), and the second dielectric film having a film thickness that is different from a film thickness of the first dielectric film (col. 8, lines 53-55).

Claims 2, 3, 12, 16, 28, 29 and 32-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuruta et al.. Tsuruta et al. discloses a semiconductor device having a non-volatile memory transistor (col. 1, lines 19-20), comprising: a first capacitor element (col. 8, line 31) and a second capacitor element (col. 8, line 39), the non-volatile memory transistor, the first and the second capacitor element being formed in one semiconductor substrate (col. 3, lines 8-10), the first capacitor element including a first lower electrode, embodied as a lower conductive film (col. 8, line 32), a first dielectric film, embodied as an insulating inter-layer film (col. 8, line 33) and a first upper electrode, embodied as an upper conductive film (col. 8, line 34), the second capacitor element having a second lower electrode, embodied as a lower conductive film (col. 8, line 41), a second dielectric film, embodied as an insulating inter-layer film (col. 8, line 43) and a second upper electrode, embodied as a upper conductive film (col. 8, line 44), and the second dielectric film having a film thickness that is different from a film thickness of the first dielectric film (col. 8, lines 53-55). Tsuruta et al. further discloses that the first dielectric film may have a plurality of

components, the second dielectric film may have a plurality of components, and that the components of the second dielectric film are different from the components of the first dielectric film (col. 6, lines 57-65).

As to claim 3, Tsuruta et al. discloses that the first and second dielectric films include an ONO film (col. 6, line 59).

As to claim 12, Tsuruta et al. discloses (col. 10, lines 15-18) that the first and the second upper electrode are formed from polysilicon.

As to claim 16, Tsuruta et al. discloses (col. 7, lines 15-19) that the first and second lower electrodes are films that are formed in the same step, and that the first and second upper electrodes are films that are formed in the same step.

As to claim 28, Tsuruta et al. discloses (col. 7, lines 1-3) that the area of the first upper electrode that faces a surface of the first dielectric film may be the same as an area of the second upper electrode that faces a surface of the second dielectric film.

As to claim 29, Tsuruta et al. discloses (col. 6, lines 66-67) that the area of the first upper electrode that faces a surface of the first dielectric film may be different from an area of the second upper electrode that faces a surface of the second dielectric film.

As to claim 32, since Tsuruta et al. discloses (col. 6, lines 66-67) that the area of the first upper electrode that faces a surface of the first dielectric film may be different from an area of the second upper electrode that faces a surface of the second dielectric film, the capacitance of the first and second capacitors would necessarily be different.

As to claim 33, capacitors are, by definition, components of analog circuits, since they can have a continuous range of capacitance values.

As to claim 34, Tsuruta et al. discloses (col. 10, lines 29-30) that the non-volatile memory transistor includes a split-gate type non-volatile memory transistor.

Allowable Subject Matter

Claims 4-11 and 17-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any

intervening claims. No prior art discloses the claimed invention in which one dielectric film includes a thermal oxide, and the other dielectric film includes a CVD oxide and a second thermal oxide.

Claims 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with upper conductive layers formed from anything other than polysilicon.

Claims 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with first and second lower electrodes formed with impurities. No prior art discloses the claimed invention with specific thickness of the first and second dielectric films.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
June 10, 2005